

ABSTRACT OF THE DISCLOSURE

A floating point flag forcing circuit comprising an circuit and a result assembler. The circuit receives a plurality of floating point operands, analyzes the floating point operand, receives one or more control input signals, determines one or more predetermined formats in which the plurality of operands are represented, and generates one or more control signals. The result assembler receives the control signals from the circuit, along with one or more inputs, and assembles a result.